Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WENGE YANG, LEWIS SHEN, and MARK CHANG

Appeal No. 2001-0607
Application No. 09/244,429

ON BRIEF

Before KRASS, FLEMING and LALL, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 18-20 and 22-25. Claims 1-17 have been withdrawn as being directed to a non-elected invention.

The invention relates to semiconductor structures. More particularly, the invention relates to etching a multilayered structure for submicron memory devices where the semiconductor

substrate is formed with a floating gate electrode, a control gate arrangement and a dielectric spacer therebetween. It is alleged that the conventional practice is to employ two different etching stages due to the inability to achieve high selectivity to polysilicon when etching the silicide. This has conventionally been compensated for by providing an undesirably thick polysilicon layer. The instant invention solves the problem and allows a reduction in the thickness of the silicide/polysilicon stack to no greater than about 800 Angstroms by the use of an etching recipe comprising chlorine and oxygen which enables the silicide and silicon layers to be etched in a single etching step with high selectivity to the underlying oxide thereby avoiding oxide damage.

Independent claim 18 is reproduced as follows:

18. A semiconductor device, comprising:

a semiconductor substrate;

an insulating layer over the semiconductor substrate;

a floating gate electrode overlying the insulating layer;

a dielectric layer substantially free of pitting therein overlying the floating gate electrode; and

a control gate arrangement directly overlying the dielectric layer wherein the control gate arrangement comprises a plurality

of silicon-based layers and has a thickness of no greater than about 800 Å.

The examiner relies on the following references:

Gluck et al.	4,923,828	May 08, 1990
Yoshimi et al.	5,290,721	Mar. 01, 1994
Prall et al.	5,345,104	Sep. 06, 1994
Yang et al.	5,973,353	Oct. 26, 1999 (filed Dec. 18, 1997)

The examiner also relies on admitted prior art [APA] depicted in Figure 2 of the instant application.

Claims 18-20, 22, 24 and 25 stand rejected under 35 U.S.C. 103 as unpatentable over Yoshimi in view of Prall and Gluck.

Claims 18-20 and 22-25 also stand rejected under 35 U.S.C. 103 as unpatentable over Yoshimi in view of APA and Gluck.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

We REVERSE.

The proper inquiry for obviousness should not be limited to the specific structure shown by the reference(s) but should be into the concepts fairly contained therein. The overriding

question to be determined is whether those concepts would have suggested to the skilled artisan the modification called for by the claims. In re Bascom, 230 F.2d 612, 109 USPQ 98 (CCPA 1956).

It is the examiner's position [answer-pages 3-4] that Yoshimi discloses a substrate 8, an insulating layer 12, a floating gate electrode 13, a dielectric layer 14 and a control gate electrode 15 of a thickness not greater than "200" [the claims recite "800"] Angstroms but that Yoshimi does not show the control gate electrode comprising a polysilicon layer with a silicide layer overlay and a dielectric free of pitting. The examiner relies on Prall's Figure 1 for the teaching of a control gate electrode with a polysilicon layer 16 overlaid with a silicide layer 17 in order to decrease sheet resistance. The examiner relies on Gluck for the teaching of forming dielectric layers free of pitting so as not to decrease dielectric strength (column 2, lines 5-6).

From these teachings, the examiner concludes that it would have been obvious to make the control gate electrode with a polysicilon layer overlaid with a silicide layer, as taught by Prall, and to form dielectric layers free of pitting, as taught by Gluck, in the device of Yoshimi in order to decrease sheet

resistance and so as not to decrease the dielectric strength of the dielectric.

With regard to the rejection of the claims relying on APA in view of Prall, the examiner makes the same allegations as before but uses APA for a teaching that "it is common (and therefore obvious) to form a control gate arrangement with a polysilicon layer 26 with a silicide layer 28 overlay and a polysilicon cap layer 30" [answer-pages 4-5].

The examiner then concludes that it would have been obvious to combine the references to Yoshimi, APA and Gluck in order to make a control gate electrode with a polysilicon layer overlaid with a silicide layer and a cap layer, as taught by APA, and to form dielectric layers free of pitting, as taught by Gluck, in the device of Yoshimi since this is common in the art and so as not to decrease strength of the dielectric.

It is our view that the examiner has not established a prima facie case of obviousness with regard to the instant claimed subject matter because the claim limitation of "wherein the control gate arrangement comprises a plurality of silicon-based layers and has a thickness of no greater than about 800 Å" is not suggested by the applied references.

The examiner apparently relies on Yoshimi for a suggestion of the claimed thickness but it is not clear as to on what, exactly, in Yoshimi the examiner is relying. After arguing that every patent is presumed valid, in response to appellants' argument that Yoshimi is not enabling, the examiner states:

> Thicknesses within range as stated by Yoshimi...are used through out the specification for other layers and, therefore, it is reasonable to assume one of ordinary skill in the art can obtain such thicknesses for the gate electrode [answer-page 7].

At page 8 of the answer, the examiner indicates that Yoshimi discloses a range of thicknesses between 15 and 3000 Angstroms. Although the examiner does not identify the portion of Yoshimi relied upon, it is clear that the examiner is citing column 1, lines 37-39, of the reference. This portion of the reference, describing the prior art to Yoshimi, calls for a second polysilicon layer to be 15-3000 Angstroms thick over the entire surface of an interlayer insulator 14 which has been grown by thermal oxidation over a floating gate pattern 13 on a gate oxide 12 which is on a substrate 8. A "resist pattern 16 is formed on the second polysilicon layer 15 to define a control gate 17, as shown in Figure 21." While Figure 21 does not show the control gate 17, it can be seen in Figure 23, where the control gate 17

and a floating gate 18 are completed with an interlayer insulating portion 19 being interposed.

The examiner is apparently relying on Yoshimi's second polysilicon layer as the claimed "control gate arrangement." However, the second polysilicon layer of Yoshimi is a single layer. Claim 18, on the other hand, requires that the control gate arrangement comprises "a plurality of silicon-based layers." Accordingly, Yoshimi's second polysilicon layer 15 cannot suggest the claimed control gate arrangement. Moreover, even if we consider resist pattern 16, together with layer 15, forming the control gate 17, to be the claimed control gate arrangement, this would clearly meet the limitation of the arrangement being comprised of a "plurality of layers," but it would not teach the claimed range, i.e., that the control gate arrangement "has a thickness of no greater than about 800 Å" because it would be pure speculation to assume that the resist layer thickness plus the second polysilicon layer 15 thickness would be less than 800 Å. Further still, the resist layer 16 is not a permanent structure since it is etched away, so it has little meaning to say that layers 15 and 16, together, form a control gate arrangement.

Still further, even if the second polysilicon layer 15 of

Yoshimi could be considered to be a "plurality of silicon-based layers," which it cannot, the examiner has picked merely one portion of the disclosed range of 15-3000 Angstroms, i.e., 15-800 Angstroms, and contended that since the claimed range is within the range disclosed by Yoshimi, the claim limitation of "the control gate arrangement comprises a plurality of silicon-based layers and has a thickness of no greater than about 800 Å" is taught by the reference. However, while Yoshimi may mention that the second polysilicon layer 15 can be 15-3000 Angstroms thick, in general, there is no specific teaching in the reference as to how a thickness of no greater than 800 Angstroms is to be achieved if, in fact, it can be achieved without appellants' disclosure. It is also interesting to note that in the example of the Yoshimi's own invention, at column 4, lines 45-46, the second polysilicon layer 15 is deposited to the extreme end of the scale, at 3000 Angstroms.

While we are also a bit skeptical on the motivation given by the examiner for combining either Prall or APA, with Gluck, with Yoshimi, to provide for the alleged deficiencies of Yoshimi, it is clear to us that there is no teaching or suggestion in the applied references for "a control gate arrangement directly overlying the dielectric layer wherein the control gate

arrangement comprises a plurality of silicon-based layers and has a thickness of no greater than about 800 Å."

With regard to the product-by-process arguments of appellants and the examiner, we agree with the examiner that a determination of patentability in "product-by-process" claims is based on product itself, even though such claims are limited and defined by process, and thus the product in such a claim is unpatentable if it is the same as, or obvious from, product of the prior art, even if the prior product was made by different process. It would not be error to affirm an examiner's rejection of "product-by-process" claims, absent proof by applicant that prior art products do not necessarily or inherently possess characteristics of his claimed product. In re Thorpe, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985).

However, the examiner must first show that the claimed structure, or the product itself, exists in the prior art. Since it is our view that the structure of claim 18, with regard to the specifically claimed control gate arrangement, has not been shown to be in the prior art or suggested by the prior art, we never get to the product-by-process claims 24 and 25.

It may be true that it is appellants' unique process which enables such a small thickness for the multi-layered control gate

arrangement to be achieved and it may be true that if the examiner can show, in the prior art, the structure set forth in claim 18, with the claimed thickness, albeit made by a different process, then the subject matter of claim 18 would be unpatentable. However, since the examiner has not shown that this structure is taught or suggested by the prior art, and we will not speculate on Yoshimi's thickness for a control gate arrangement and on whether it can be made of a plurality of layers, we will not sustain the examiner's rejection of claims 18-20 and 22-25 under 35 U.S.C. 103.

The examiner's decision is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES

)
)
PARSHOTAM S. LALL)
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